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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Daniel R. Knebel,et al.

Examiner: Ferris

Serial No.: 09/406,663

Art Unit: 2123

Filed: September 27, 1999

Docket: YOR919990438US1 (13031)

For: SYSTEM AND METHOD FOR VLSI VISUALIZATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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DECLARATION UNDER 37 C.F.R. §1.312

Dear Sir:

I, Daniel R. Knebel, Declare that:

1. I am a co-applicant of the above-identified patent application and a co-inventor of the subject matter disclosed and claimed in the patent application, and I am submitting this Declaration in response to the Office Action dated March 12, 2003 issued in the application.

2. In the Office Action, the Examiner rejected Claims 1-7 and 10-42 as being fully anticipated by an article "Diagnosis and Characterization of Timing-Related Defects by Time-Dependent Light Emission."

3. I am a co-author of this article and am personally familiar with the circumstances of the publication of the article.

4. This article was first published in October 1998 in the proceedings of the International Test conference, and the article was not publicly available before that first publication. A copy of the cover page of the proceedings is submitted herewith as Exhibit B.

5. This article includes a footer "0-7803-5092-8/98." It is my understanding that this footer is an article code from the Copyright Clearance Center, which, I believe, handles fee collection for these articles. The codes apparently were generated before printing of the proceedings.

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June 11, 2003

Dated

Daniel R. Knebel

DIAGNOSIS AND CHARACTERIZATION OF TIMING-RELATED DEFECTS BY TIME-DEPENDENT LIGHT EMISSION

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Abstract- Technological advances such as flip-chip packaging, multiple hierarchical wiring planes, and ultra-high frequencies reduce the effectiveness of conventional diagnostic techniques. It has recently been demonstrated that light pulses emitted during circuit switching can be used to characterize the behavior of integrated circuits. In this paper, a new method of circuit characterization using this technique is described. An example of the diagnosis of a timing failure caused by a resistive path to a single transistor is described.

I. Introduction

Increasing design complexity and shrinking device dimensions are forces driving the need for improved diagnostic methods for IC failure analysis [1-2]. Improved software methods are becoming available, but require that the circuit be designed for diagnostics.

Many of the classical hardware failure analysis techniques are losing their effectiveness [3-4]. For example, electron beam testing has been widely used for precise timing characterization of the internal circuitry of ICs. Increasing numbers of wiring planes, widespread use of power planes for electro-magnetic isolation, and a trend toward flip-chip technology, however, reduce the effectiveness of this technique. In many cases, it has become obsolete altogether.

At the same time, increasing device speeds and operating frequencies may make such characterization more important. As circuit speeds approach and exceed 1 GHz, effects that have normally been ignored, such as net-to-net coupling, precise clock skew, and di/dt voltage degradation must now be modeled and precisely characterized. It also becomes more likely that a subtle defect, such as a resistive via, will cause a timing failure.

Lower capacitance related to smaller feature sizes and faster devices will have a tendency to reduce the effectiveness of capacitive probing techniques. Also related to higher device speeds are increased use of low threshold devices and decreasing supply voltage. These trends may decrease the effectiveness of certain IDDq tests due to higher background currents.

Static light emission techniques (photon emission microscopy) can be used to locate defects which cause steady state current to leak through CMOS transistors, such as would be found with IDDq testing. These static techniques have recently been extended to work from the

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backside of the IC [9-10]. Static light emission techniques, however, provide no timing related information.

Device characterization through the analysis of dynamic light emission can be performed from the backside of the IC and provides the timing resolution needed to diagnose current and future ICs. It is such a method, which has been named Picosecond Imaging Circuit Analysis (PICA), that is described in the following.

II. Background

IBM researchers have demonstrated the ability to measure optical emission of normally biased CMOS logic gates, which occurs only in a short period during the switching transient. The time response of the measuring system is less than 100 psec (FWHM).

Because a portion of the emission is below the band gap of Si, measurement is possible through a lightly doped substrate. While charge coupled devices (CCD's) are capable of spatial resolution of such emission, their time response is too slow to resolve the short switching transients of CMOS devices, which are on the order of 10-100 psec.

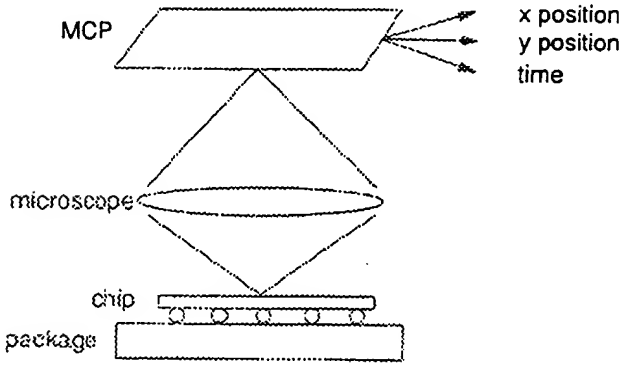

Figure 1. Schematic diagram of PICA measuring apparatus for backside analysis.

As shown in Figure 1, a thermoelectrically cooled microchannelplate (MCP) photomultiplier with a position sensitive resistive anode is implemented to provide both spatial and temporal resolution. A portion of the IC sample is imaged with a microscope onto the photomultiplier and conversion electronics store position and time (x,y,t) information.

PICA techniques are now being developed to perform detailed device characterization and failure analysis through the backside of an IC mounted on a flip-chip carrier. Because much of the emitted light in the detectable spectral range can be absorbed by a substrate, the sample to be tested is first thinned and the surface polished to an optical finish. Thinning is preferably performed without removing the IC from its usual packaging. Suitable temporary chip carriers, however, are often available.

In parallel with sample preparation, test patterns are generated to stimulate the sample, and devices of interest ar identified and physically located in the design layout. For failure analysis applications the exact location of the failure is typically not known. Software diagnostics are employed to predict the most likely locations of the source of the failure.

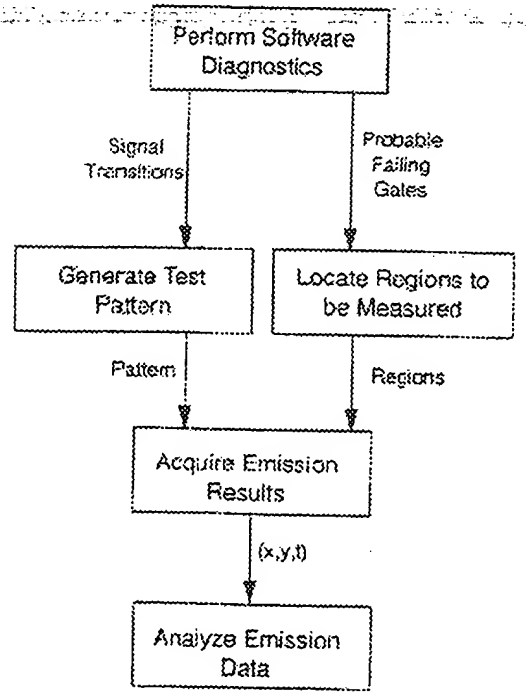

Figure 2. Flow diagram of diagnostic procedure

Because PICA uses standard infrared optics, various microscope objectives are used to image large or small portions of the device under test. At lower powers, rough imaging may be employed to collect switching data for a large number of devices. Such an image may be used to eliminate a number of the possible failure modes suggested by diagnostic analysis. Using a high power objective measures fewer devices at one time, but provides the spatial resolution needed to determine the switching behavior of individual (minimum dimension) transistors.

Collected images are post-processed to provide insights into the device operation. Integration of the measured data over time creates an "emission photograph" similar to that measured with a CCD. Selection of a single emission "spot" in the (x,y) plane of the collected image and plotting the time dependence of the emission intensity of the spot yields an optical waveform of the emission of the transistor or transistors in the spot.

Layout to schematic mapping may be used to relate such waveforms to schematic elements and provides a means for comparison to simulation. Circuit delays and logic evolution can be deduced directly from the waveforms. The data may even be organized into time-resolved emission images. When displayed sequentially, these images provide a movie-like recreation of the switching activity in the field of view.

III. PICA Applications

Dynamic light emission for failure analysis and characterization has been demonstrated on various samples. Applications which have been demonstrated are described briefly below. A specific example is described in more detail in the next section.

•Diagnosis of timing-only failures

Failures that cause faulty operation only at or near maximum device operating speed can be diagnosed by measuring emission of a selected field of view and calculating circuit element delays. The results may be used to reveal races or long paths that cause a fault to occur. The application described in the next section is an example of a timing-only failure diagnosed with PICA.

•Analysis of IDDq-only failures

IDDq-only failures may be due to a number of causes, such as bridge faults, shorts through thin oxide, and leaking devices. Characterization of these failures would be useful to determine the effectiveness of the IDDq test and to improve its coverage and device yield. A circuit containing an intentionally placed defect was analyzed and demonstrates this capability.

The defective circuit passed all logical tests, but had abnormally high IDDq. PICA measurements were used to locate the short and to quantify additional circuit delay caused by the defect (140 psec). This behavior was also verified using and EBEAM tool.

• Detailed delay characterization

The capability to resolve path delays to 10-20 psec has been demonstrated [13]. Detailed simulation of a ring oscillator provided a list of inverter delays differing only due to small variations in wire and fanout loading. Measurements taken on a sample of the ring oscillator provided a means to determine the precision and accuracy of the current PICA apparatus.

• Clock skew analysis

An analysis of clock distribution on a large microprocessor was made to determine offset between the chip reference clock and the receiver of the off-chip clock and skew between the fanout buffers that drive the processor memory elements.

IV. Example Application in Failure Analysis

An example of using PICA for failure analysis is taken from a yield learning cycle of a recent CMOS process. A high D.C. (stuck-fault) yield had already been calculated from wafer level test statistics, but module level testing of a microprocessor revealed timing related failures. Root-cause

analysis was performed on selected samples to determine sources of the timing failures.

Diagnostics generated from at-speed electrical testing were used to predict possibly faulty circuit elements. A sample with a timing related failure in a register file was selected for PICA analysis.

The probable fault location in the register file had been isolated using software diagnostics to a particular latch pair, which could be stimulated repeatedly at high frequency. A portion of the schematic diagram is shown in Figure 3.

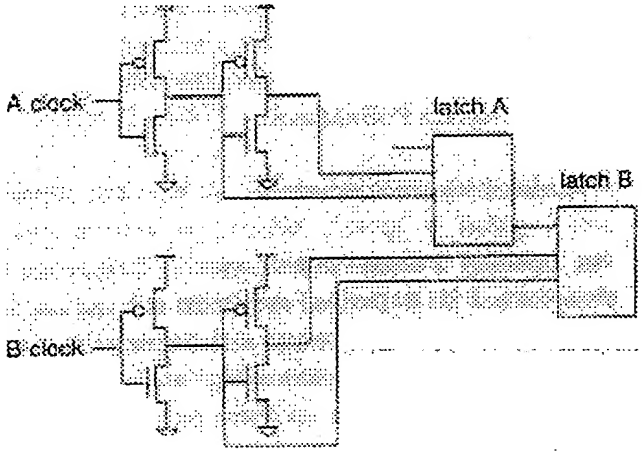

Figure 3. Schematic diagram of suspected faulty circuit

Verification of the faulty circuit, analysis of the defect, and refined location were the goals of the analysis. As the part was being prepared, the layout was compared to the schematic to determine device correspondence and a test pattern was devised to stimulate the circuit.

Simulation of the good circuit model was made to predict both the static emission pattern of the register file and a time-resolved emission waveform for a latch pair. Figure 4 shows the clock sequence used to scan an alternating pattern of zero's and one's through the register file. The simulated current waveform for a single latch pair is shown relative to the clocks. Locations of the peaks in the current waveform predict the occurrence of light emission.

Figure 5 shows results of a measurement using PICA. At the top of the figure is a time integrated emission pattern with an arbitrary latch pair circled. The time-resolved emission waveform of the circled latches is plotted in the lower section of the figure. The emission waveform represents emission intensity vs. time for all of the transistors in the latch pair.

The locations of the emission spikes compare favorably with the predicted emission pattern and coincide with the launch and capture times determined by the rising and falling edges of the clocks.

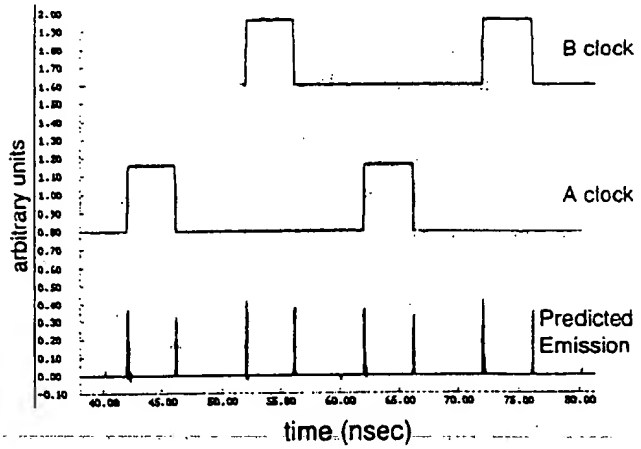

Figure 4. Predicted emission waveform for a good latch pair.

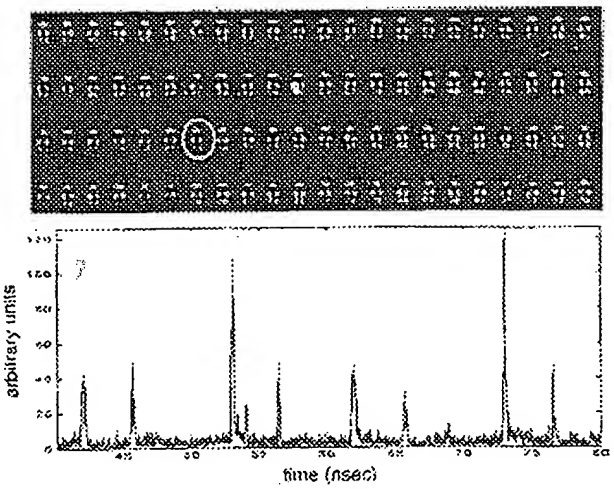

Figure 5. Measured emission waveform for a good latch pair.

The time-resolved emission waveform of the suspected faulty circuit was extracted in a similar fashion. Figure 6 shows the time integrated image with the faulty latch pair circled and its corresponding emission waveform. Relatively high emission intensity observable in the circled area is an indication that the circuit was correctly identified as the source of the failure. Information extracted from the emission waveform was used to verify the anticipated additional delay due to the defect and to discover a relationship to the B clock.

Comparing the emission waveform shown in Figure 6 with the clock sequence (see Figure 4) reveals that excess emission occurs only when the B clock is active (high). The excess emission occurs in both clock cycles shown (the first cycle is storing a zero and the second cycle is storing a one). This ability to correlate emission data with circuit timing is a critical element that sets PICA apart from static-emission analysis.

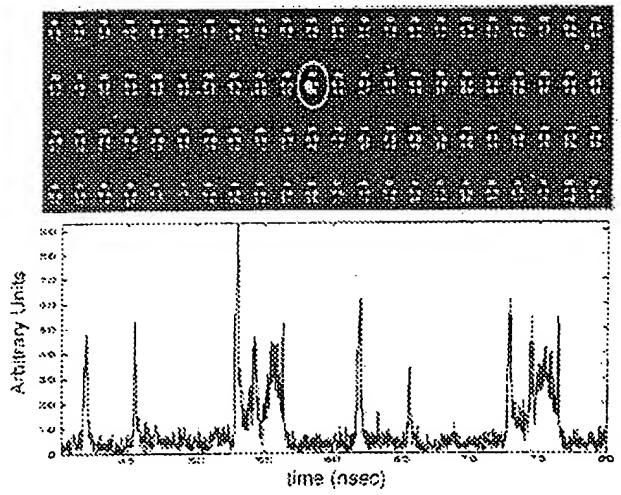

Figure 6. Measured emission waveform for the defective latch pair.

Of the suspected defect types and locations, only one could produce such a signature: a series resistance between the B clock input and the pull-up of the first inverter in the circuit. A resistor representing the defect is shown schematically in Figure 7.

The simulated waveform matches the signature of the measured optical waveform and is shown in Figure 8. A second PICA measurement using a higher power objective would have been able individually resolve the malfunctioning transistor, but the time-resolved data had already pinpointed the location of the failure. In the interest of time, physical failure analysis was begun. The defect was indeed identified at the suspected location. Figure 9 shows low and high magnification scanning-electron microscope (SEM) images of the defect, which is located with the arrow.

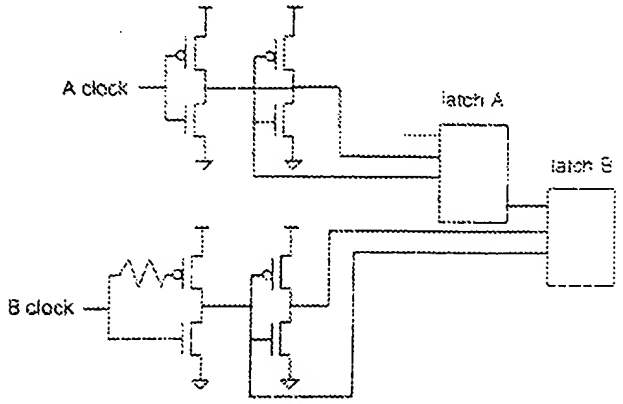

Figure 7. Schematic diagram with series resistor depicting defect.

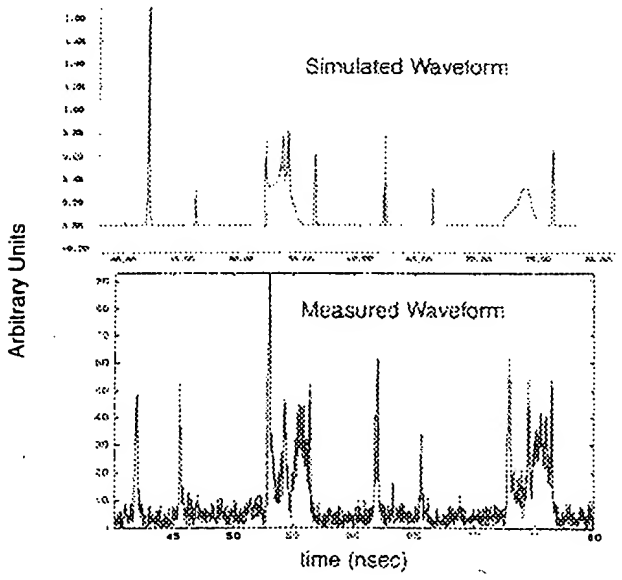

Figure 8. Simulated and measured emission waveforms of defective circuit.

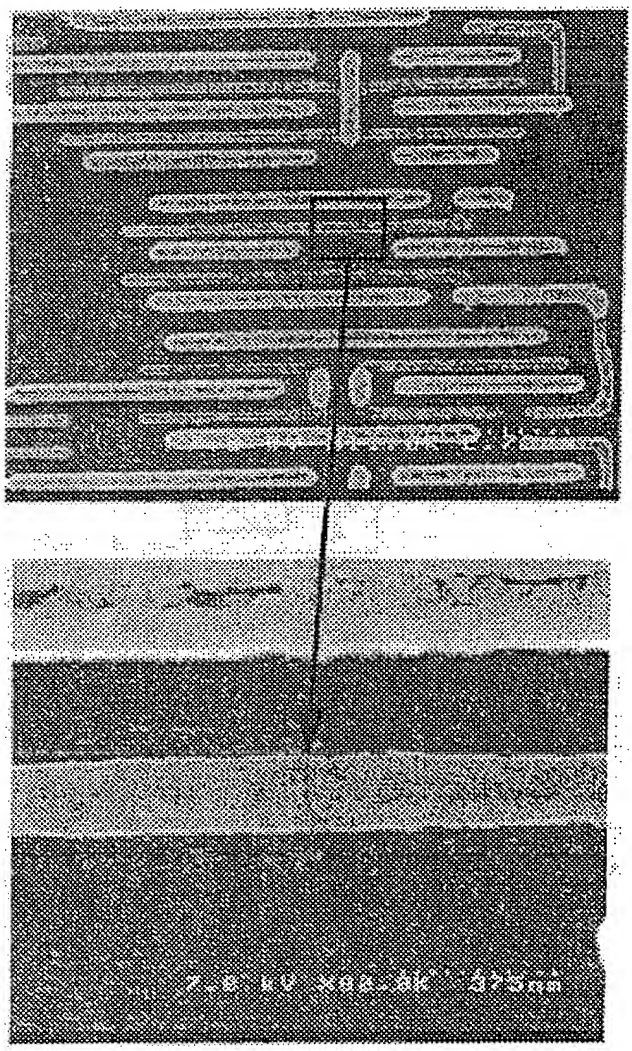

Figure 9. Micrographs of defect.

V. Conclusions

PICA is a totally noninvasive method for measuring switching activity in CMOS ICs. It is capable of detecting switching activity through the backside or frontside of a chip with temporal resolution in the picosecond range. Spatial and temporal data for numerous transistors is gathered in a single image and can be stored for off-line analysis making PICA a highly productive analytical tool.

The full range of applications suitable to the technique has yet to be determined, but demonstrations of its strength as a characterization and failure analysis tool have already been made. Localization of timing-related defects and analysis of subtle IDDq-only or at-speed only failures are both high leverage needs and solvable with the technique. As the operating speed of ICs increase and operating margins shrink, subtle timing-only defects will begin to dominate, challenging many current fault isolation methods.

Fault localization is a critical step in the process of analyzing a failure to its root cause. PICA provides a means for both rough and fine defect localization, as well as defect-related timing characterization. While localization of stuck-faults is possible, PICA is most particularly suited to analysis of failures that have fewer, if any, software diagnostic tools available for analysis. It has been shown to be effective in detailed characterization of a timing-only defect.

Subtle defects that cause IDDq-only failures, or at-speed only failures are becoming more difficult to screen from good parts. PICA provides a robust means for diagnosing line and field returns to aid in the root-cause analysis of such defects. An objective of the development of the technique is to improve debug turn-around-time to meet the needs of yield learning (e.g., real time analysis).

VI. Acknowledgments

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